

WHAT IS CLAIMED IS:

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1. A packet processing apparatus, comprising:
a distributor for assigning a sequence number to each
of a plurality of packets input to said distributor and
distributing the packets;

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a plurality of packet analyzing units for realizing
parallel execution of information analyzing processes on
the packets distributed from the distributor;

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an order correction unit for receiving the packets
from the packet analyzing units, rearranging the packets
in order according to the sequence number assigned to each
of the packets, and outputting the packets in the rearranged
order.

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2. The packet processing apparatus as claimed in
claim 1, wherein:

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the distributor distributes the packets to the packet
analyzing units according to a value of a predetermined bit
in each of the packets input to said distributor.

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3. The packet processing apparatus as claimed in
claim 1, wherein:

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the distributor includes a plurality of output
buffers to which the packets are distributed, said
plurality of output buffers being arranged corresponding
to the packet analyzing units; and

the distributor sets a threshold value to an amount

of accumulated data in each of the output buffers, and stops distributing the packets to at least one of the output buffers when the amount of accumulated data in said at least one of the output buffers exceeds the threshold value.

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4. The packet processing apparatus as claimed in
10 claim 1, wherein the order correction unit includes:

a packet buffer for storing the packets supplied from the packet analyzing units;

an address manager having a plurality of entries
corresponding to the sequence numbers assigned to the
15 packets; and

a buffer control unit for storing, in the entries of the address manager, packet buffer addresses of the packets supplied from the packet analyzing units and stored in the packet buffer, which packet buffer addresses are stored in
20 the entries according to the sequence number assigned to each of the packets; reading the packet buffer addresses from the entries of the address manager in order according to the sequence number assigned to each of the packets; reading the packets from the packet buffer in order
25 according to the sequence numbers; and outputting the packets in the read order.

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5. The packet processing apparatus as claimed in claim 4, wherein:

the packet buffer addresses are read from the address manager by the buffer control unit after the packet
35 addresses have been stored in all the entries of the address manager.

5 6. The packet processing apparatus as claimed in
claim 5, wherein:

 the order correction unit includes a first
dysfunction detector for detecting a dysfunction when a
difference between the number of packets stored in the
packet buffer and the number of packets read from the packet
10 buffer exceeds a predetermined value.

15 7. The packet processing apparatus as claimed in
claim 4, wherein:

 the order correction unit includes a second
dysfunction detector for detecting a dysfunction when the
entry of the address manager in which the packet buffer
20 address has just been stored is ahead of the entry from which
the packet buffer address is to be read by more than a number
of entries corresponding to a predetermined monitoring
window value.

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 8. The packet processing apparatus as claimed in
claim 7, wherein:

30 after the second dysfunction detector detects the
dysfunction, the order correction unit resumes reading the
packet buffer addresses from the address manager starting
from the earliest entry of an unbroken succession of entries
storing the packet buffer addresses, tracking back from the
35 entry in which the packet buffer address has most recently
been stored.

5 9. The packet processing apparatus as claimed in
claim 1, further comprising:

search means for integrally performing search
processes requested by the packet analyzing units.

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10. The packet processing apparatus as claimed in
claim 9, wherein:

15 the search means has a function of mediating accesses
made by the packet analyzing units.

20 11. The packet processing apparatus as claimed in
claim 9, wherein:

the search means is arranged to execute the search
processes using an associative memory.

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12. The packet processing apparatus as claimed in
claim 11, wherein:

30 the search means is arranged to calculate a number
of hits made for each of entries provided in the associative
memory.